IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNITED STATES RECEIVING OFFICE

#3/0

Applicant(s)	:	McCORD, Don
Serial No.	:	New application (to be assigned)
Filing Date	:	Herewith
International Application No.:		PCT/US01/05455
International Filing Date	:	21 February 2001
Title	:	METHOD AND SYSTEM FOR WAFER AND DEVICE-LEVEL TESTING OF AN INTEGRATED CIRCUIT
Attorney Docket No.	:	37802PCT-US

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

This Amendment is submitted together with a Transmittal Letter concerning a filing under 35 U.S.C. § 371 based on PCT application serial number PCT/US01/05455 filed on 21 February 2001.

Please amend this national stage application identified above as follows:

CERTIFICATE OF MAILING BY "EXPRESS MAIL" UNDER 37 CFR § 1.10

"Express Mail" mailing label number: EF272757617US Date of Mailing: October 19, 2001

I hereby certify that the application/correspondence attached hereto is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Box PCT, Assistant Commissioner for Patents, Washington, D.C. 20231.

KHIM DeCORD
Typed name of person mailing paper or fee

Signature of person mailing paper or fee

IN THE SPECIFICATION:

Please add at page 1, line 1:

This national stage application claims the benefit of:

U.S. Provisional Application No. 60/184,192, filed on 22 February 2000, and entitled "*Method and Apparatus for Wafer and Device Level Testing for an RSL Logic Device*," and

U.S. Provisional Application No. 60/234,647, filed on 22 September 2000, and entitled "*Memory Tester Architecture.*"

Respectfully submitted,

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Telephone: (512) 343-6116

ATTORNEY FOR APPLICANT

REDACTED SPECIFICATION

Please add at page 1, line 1:

This national stage application claims the benefit of:

U.S. Provisional Application No. 60/184,192, filed on 22 February 2000, and entitled "*Method and Apparatus for Wafer and Device Level Testing for an RSL Logic Device*," and

U.S. Provisional Application No. 60/234,647, filed on 22 September 2000, and entitled "*Memory Tester Architecture.*"